CLAIMS

What is claimed is:

1. A pulsed current generator circuit comprising:

a) a current source for applying a current to a device under test,

b) a controlled current shunt for shunting current from the device under test, and

c) a booster circuit for supplying a booster current to the device under test when the controlled current shunt is opened and current again flows through the device under test, thereby facilitating recharge of a parasitic capacitance associated with the device under test.

2. The pulsed current generator circuit as defined by claim 1 wherein the booster circuit comprises an NMOS transistor serially connected with a PMOS transistor between a voltage potential and the parasitic capacitance,

a capacitor shunting the NMOS transistor for providing a DC voltage at a common point of the NMOS transistor and the PMOS transistor, and

control circuitry coupled to receive a shunt control signal and in response thereto control conduction on the PMOS transistor and provision of the booster current.

3. The pulsed current generator circuit as defined by claim 2 wherein the DC voltage at the common point is approximately equal to the desired voltage on the parasitic capacitor.

4. The pulsed current generator circuit as defined by claim 3 wherein the booster circuit includes bias circuitry for the NMOS transistor and PMOS transistor whereby bias voltage on the PMOS transistor is larger than the bias voltage on the NMOS transistor by a voltage increment, Δ, whereby both transistors are not conductive during steady state conditions.

5. The pulsed current generator circuit as defined by claim 4 wherein the bias circuitry comprises first and second operational amplifiers responsive to a fixed voltage, V_b, and a variable voltage, Vbst.

6. The pulsed current generator circuit as defined by claim 4 wherein the bias circuitry comprises an operational amplifier responsive to a voltage between two fixed voltages of

same voltage magnitude and opposite polarity and a variable voltage, Vbst, where Vbst biases the NMOS transistor and the operational amplifier biases the PMOS transistor.

7. The pulsed current generator circuit as defined by claim 4 and including a resistor connecting the PMOS transistor to the device under test to limit boosting current.

8. The pulsed current generator circuit as defined by claim 4 wherein the control circuitry includes cascade buffers for inverting and delaying input signals applied thereto, one buffer controlling the application of a conduction bias to the PMOS transistor in response to the shunt control signal switching to a voltage level to open the controlled current shunt.

9. The pulsed current generator circuit as defined by claim 2 and including a resistor connecting the PMOS transistor to the device under test to limit boosting current.

10. The pulsed current generator circuit as defined by claim 2 wherein the control circuitry includes cascade buffers for inverting and delaying input signals applied thereto, one buffer controlling the application of a conduction bias to the PMOS transistor in response to the shunt control signal switching to a voltage level to open the controlled current shunt.